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Paper No. 9
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

SAMSUNG ELECTRONICS COMPANY, LTD.,
Patent Owner.

Case IPR2016-00134
Patent 8,252,675 B2

Before JAMESON LEE, PATRICK R. SCANLON, and JUSTIN BUSCH, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108(a)

I. INTRODUCTION

A. Background

On November 4, 2015, a Petition (Paper 2, "Pet.") was filed to institute *inter partes* review of claims 1–8 and 10–15 of U.S. Patent No. 8,252,675 B2 (Ex. 1101, "the '675 patent"). Patent Owner filed a Preliminary Response (Paper 6, "Prelim. Resp.") on February 16, 2016.

Institution of *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(a). In the circumstances of this case, as explained below in Section II-A, we exercise our discretion to not institute *inter partes* review on any of claims 1–8 and 10–15 of the '675 patent on any ground. Additionally, in the alternative, and as explained below in Section II-B, we reject the petition because substantially the same prior art previously was presented to the Board, by Petitioner, in IPR2015-01318. *See* 35 U.S.C. § 325(d).

B. Related Matters

The parties indicate that the '675 patent is at issue in *Samsung Electronics Co., Ltd. v. NVIDIA Corp.*, 3:14-cv-00757-REP (E.D. Va.). Papers 2, 5. The parties also indicate that the '675 patent was at issue in IPR2015-01318.[1] *Id.*

C. The '675 Patent

The '675 patent relates to a method of forming an insulated-gate transistor (independent claim 1) and a method of forming an integrated circuit device (independent claim 6). The Background of the Invention

[1] On December 7, 2015, the Board denied institution of *inter partes* review of the '675 patent in IPR2015-01318.

portion of the Specification does not articulate any problem with prior art methods, and the Summary portion of the Specification does not articulate what objective or advantage is achieved by the invention, relative to prior art methods. The Background of the Invention portion states:

> MOS transistors are classified as n-MOS transistors or p-MOS transistors in accordance with the channel type which is induced beneath the gate electrode. The gate electrodes of the n-MOS transistor and the p-MOS transistor may be formed of different metals so that the n-MOS transistor and the p-MOS transistor have different threshold voltages.

Ex. 1101, 1:24–30. None of the independent claims at issue requires the formation of both an n-MOS and a p-MOS transistor, much less an n-MOS and a p-MOS transistor that have respectively different threshold voltages. Independent claims 1 and 6 each require a metal gate electrode that itself comprises multiple metal layers, and claim 6 additionally specifies that the gate electrode is that of a PMOS transistor.

Aside from requiring multiple metal layers in the gate electrode, each of claims 1 and 6 requires formation of a dummy gate electrode, removal of the dummy gate electrode, and then the formation of a new metal gate electrode by deposition of multiple additional metal layers. Those additional metal layers are referred to in claim 1 as first metal layer and second metal layer, and in claim 6 as second metal gate electrode layer and third metal gate electrode layer.

Of all the challenged claims, claims 1 and 6 are the only independent claims. They are reproduced below:

1. A method of forming an insulated-gate transistor, comprising:

forming a gate insulating layer on a substrate;
forming a metal buffer gate electrode layer on the gate insulating layer;

forming a dummy gate electrode layer on the buffer gate electrode layer, said dummy gate electrode layer and said buffer gate electrode layer comprising different materials;

patterning the dummy gate electrode layer and the buffer gate electrode layer in sequence to define buffer gate electrode on the gate insulating layer and a dummy gate electrode on the buffer gate electrode;

forming electrically insulating spacers on sidewalls of the dummy gate electrode and on sidewalls of the buffer gate electrode;

covering the spacers and the dummy gate electrode with an electrically insulating mold layer;

removing an upper portion of the mold layer to expose an upper surface of the dummy gate electrode;

removing the dummy gate electrode from between the spacers by selectively etching back the dummy gate electrode using the mold layer and the spacers as an etching mask;

depositing a first metal layer onto an upper surface of the mold layer and onto inner sidewalls of the spacers and onto an upper surface of the buffer gate electrode;

filling a space between the inner sidewalls of the spacers by **depositing a second metal layer** onto a portion of the first metal layer extending between the inner sidewalls of the spacers to thereby **define a metal gate electrode**

comprising a composite of the second metal layer, a portion of the first metal layer having a U-shaped cross-section and the buffer gate electrode.

Id. at 10:59–11:26 (emphases added).

6. A method of forming an integrated circuit device, comprising:

forming a gate insulating layer on a substrate;

forming a first metal gate electrode layer on the gate insulating layer;

forming a dummy gate electrode layer on the first metal gate electrode layer, said dummy gate electrode layer and said first metal gate electrode layer comprising different materials;

patterning the dummy gate electrode layer and the first metal gate electrode layer in sequence to define a dummy gate electrode on the patterned first metal gate electrode layer;

forming electrically insulating spacers on sidewalls of the dummy gate electrode and on sidewalls of the patterned first metal gate electrode layer;

removing the dummy gate electrode from between the spacers by selectively etching back the dummy gate electrode using the spacers as an etching mask;
depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer,
depositing a third metal gate electrode layer onto the second metal gate electrode layer to thereby fill a space between the inner sidewalls of the spacers, said second and third metal gate electrode layers comprising different materials;

planarizing the third metal gate electrode layer and the second metal gate electrode layer to thereby **define a composite metal**

> **gate electrode** of a PMOS transistor between the inner sidewalls of the spacers, **said composite metal gate electrode comprising a portion of the third metal gate electrode layer, a portion of the second metal gate electrode layer having a U-shaped cross-section and the patterned first metal gate electrode layer**.

Id. at 11:39–12:11 (emphases added).

D. Evidence Relied Upon

Petitioner relies on the following reference:[2]

Reference		Date	Exhibit
Hsu	U.S. Patent No. 8,536,660 B2	Sept. 17, 2013	Ex. 1105

E. The Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

Reference	Basis	Claims Challenged
Hsu	§ 102(e)	1–8 and 10–15
Hsu	§ 103(a)	12

II. ANALYSIS

A. Discretionary Non-Institution

Institution of *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(a). Among the factors we consider in deciding whether to exercise discretion not to institute review are:

[2] Petitioner also relies on the Declaration of Jack Lee, Ph.D. (Ex. 1103).

(1) the finite resources of the Board;

(2) the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review;

(3) whether the same petitioner already previously filed a petition directed to the same claims of the same patent;

(4) whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known about it;[3]

(5) whether at the time of filing of the second petition the petitioner already received patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition;[4]

(6) the length of time that elapsed between the time petitioner learned of the prior art asserted in the second petition and filing of the second petition; and

(7) whether petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent.

We are concerned about the limited resources of the Board and fundamental fairness for both Petitioner and Patent Owner. Petitioner cannot expect automatic acceptance of multiple petitions for

[3] *See Conopco, Inc. v. Proctor & Gamble Co.*, Case IPR2014-00506, slip op. at 4 (PTAB Dec. 10, 2014) (Paper 25) (Informative), and slip op. at 6 (PTAB July 7, 2014) (Paper 17); *Toyota Motor Corp. v. Cellport Sys., Inc.*, Case IPR2015-01423, slip op. at 8 (PTAB Oct. 28, 2015) (Paper 7).

[4] *See Conopco, Inc. v. Proctor & Gamble Co.*, Case IPR2014-00628, slip op. at 11 (PTAB October 20, 2014) (Paper 21) (discouraging filing of a first petition that holds back prior art for use in later attacks against the same patent if the first petition is denied); *Toyota Motor Corp.*, slip op. at 8 ("the opportunity to read Patent Owner's Preliminary Response in IPR2015-00634, prior to filing the Petition here, is unjust.").

consideration, if they are against the same claims of the same patent and filed so long apart that Petitioner received the benefit of having studied Patent Owner's Preliminary Response in the first petition or the Board's decision on whether to institute review in the first petition, prior to filing the second petition. That is especially so if Petitioner, at the time of filing of the first petition was aware of or should have been aware of the prior art references applied in the second petition.

The potential inequity based on a petitioner's filing of serial attacks against the same claims of the same patent, while having the opportunity to adjust litigation positions along the way based on either patent owner's contentions responding to prior challenges or the Board's decision on prior challenges, is real and cannot be ignored. This is not to say, however, that multiple petitions against the same claims of the same patent are never permitted. Rather, each case depends on its own facts. We look to and consider, in each case, as we do here, what rationale a petitioner offers for filing multiple petitions and for the time elapsed between those filings.

The instant Petition is the second petition filed by Petitioner challenging claims 1–8 and 10–15 of the '675 patent. The first such petition was filed on June 1, 2015, in IPR2015-01318, alleging that: (1) claims 1–8 and 10–15 are unpatentable as anticipated by U.S. Pub. App. No. 2009/0065809 A1 ("Yamakawa"); and (2) claim 9 of the '675 patent is unpatentable as obvious over Yamakawa and U.S. Patent No. 8,339,381 ("Yeh"). On September 10, 2015, in IPR2015-01318, Patent Owner filed a

preliminary response that argued that the petition in that proceeding was deficient on the merits.

Approximately two months later, on November 4, 2015, Petitioner filed the second petition, i.e., the Petition in this proceeding. Paper 2. In this Petition, Petitioner asserts that (1) claims 1–8 and 10–15 are unpatentable as anticipated by Hsu; and (2) claim 12 of the '675 patent is unpatentable as obvious over Hsu. In the Petition, Petitioner states:

> Petitioner was unaware of the Hsu reference when the previous petition, No. IPR2015-01318, was filed on June 1, 2015.

Paper 2, 3. Petitioner reiterates:

> At the time the previous petition [(IPR2015-01318)] was filed, neither Petitioner nor its expert, Dr. Jack Lee had knowledge of Hsu.

Id. at 9. The Petition states nothing about when Petitioner learned of Hsu or how it became aware of Hsu.

In the Preliminary Response, Patent Owner provides much of the pertinent information surrounding Petitioner's discovery of Hsu. Patent Owner points out that Petitioner's representation that Petitioner was unaware, at the time of filing of the petition in IPR2015-01318 (June 1, 2015), of the prior art reference Hsu is incorrect. Prelim. Resp. 4–5. Patent Owner states:

> But both Petitioner and its counsel were, in fact, aware of Hsu prior to June 1, 2015. In particular, in an ITC proceeding (No. 337-TA-941) also involving Petitioner and Patent owner, Petitioner produced *Hsu* (Ex. 2002, bearing production number NV941-ITC-000104802-820) on May 8, 2015 – i.e., prior to June 1, 2015 when Petitioner filed the first petition. (Ex. 2001 at 1, setting forth a range of production numbers that includes production number NV841-ITC-000104802-820 corresponding to *Hsu*). Moreover, Petitioner is represented by the same law

> firm (Latham & Watkins) in both the aforementioned ITC proceeding and the instant proceeding. In fact, all three attorneys listed as Petitioner's counsel in the instant proceeding are also Petitioner's counsel of record in the ITC proceeding. (Pet. at 1; Exs. 2003, 2004.) While the ITC proceeding does not involve the '675 patent, it is part of the ongoing dispute between Petitioner and Patent owner that spans the ITC and federal district courts. Moreover, the patents involved in both the ITC proceeding and the district court proceeding in which the '675 patent is asserted relate to semiconductor devices.

According to Patent Owner, Hsu was a reference identified and produced by Petitioner to Patent Owner during litigation between Petitioner and Patent Owner before the International Trade Commission approximately one month prior to the filing, on June 1, 2015, by Petitioner of the petition in IPR2015-01318 against the '675 patent. Hsu was not one of numerous prior art references provided to Petitioner, the individual relevance of which had to be subsequently analyzed and determined. Rather, according to Patent Owner, Hsu was a prior art reference identified and produced by Petitioner.

Patent Owner's contention is at odds with Petitioner's express representation in the Petition (Paper 2 at 3, 9) that prior to filing its first petition against the '675 patent in IPR2015-01318, on June 1, 2015, it was unaware of Hsu. A telephone conference call was held on March 1, 2016. The participants of the call were respective counsel for the parties and Judges Lee, Scanlon, and Busch. During the conference call, counsel for Petitioner indicated that Petitioner does not factually dispute Patent Owner's account of how the Hsu reference was produced in related ITC litigation. *See* Paper 8. Thus, on this record, the statements in the Petition that at the time of filing of the first petition in IPR2015-01318 Petitioner was unaware

of Hsu is incorrect, and Petitioner has acknowledged that incorrect statement.

On this record, one remaining question is why Petitioner did not assert Hsu against the '675 patent until more than five months after filing of the first petition against the '675 patent in IPR2015-01318, and approximately two months after Patent Owner filed its preliminary response in IPR2015-01318. Petitioner offered no explanation in its Petition.

Although Petitioner did request to file a reply to Patent Owner's Preliminary Response, the request was to address two alleged "misstatements" by Patent Owner in the Preliminary Response, not to acknowledge its own misstatement in the Petition that Petitioner was not aware of Hsu at the time of filing of the petition in IPR2015-01318, and not to explain why Hsu was not asserted in the first petition. Paper 8. More importantly, during the conference call on March 1, 2016, counsel for Petitioner expressed that Petitioner does not dispute Patent Owner's representation that Petitioner identified and produced Hsu, on May 8, 2015, in related litigation between Petitioner and Patent Owner before the International Trade Commission, about one month prior to filing of the petition in IPR2015-01318. *Id.*

Given the undisputed facts as noted above, it would be unjust to Patent Owner to institute review in this proceeding. Petitioner has provided no rationale on why it waited until November 4, 2015, more than five months after filing of the first petition on June 1, 2015, in IPR2015-01318, to file the Petition in this proceeding, given that Petitioner was aware of Hsu at least by May 8, 2015. Notably, in IPR2015-01318, Patent Owner's preliminary response was filed on September 10, 2015. On the other hand,

not instituting review in this proceeding would not be unjust to Petitioner, because Petitioner was aware of Hsu when the first petition was filed on June 1, 2015, in IPR2015-01318, and subsequently waited too long to file the second petition relying on Hsu with no apparent justification.

Under the circumstances of this case, as explained above, we hold Petitioner accountable for its own actions and inactions. Given the limited resources of the Board, we exercise our discretion not institute review in this proceeding, which is the second petition filed by Petitioner against claims 1–8 and 10–15 of the '675 patent. *See* 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(a).

B. Separate Reasoning under 35 U.S.C. § 325(d)

In addition to the foregoing, we also decline to institute *inter partes* review based on consideration of 35 U.S.C. § 325(d), which provides:

> MULTIPLE PROCEEDINGS.—Notwithstanding sections 135(a), 251, and 252, and chapter 30, during the pendency of any post-grant review under this chapter, if another proceeding or matter involving the patent is before the Office, the Director may determine the manner in which the post-grant review or other proceeding or matter may proceed, including providing for the stay, transfer, consolidation, or termination of any such matter or proceeding. **In determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.**

(Emphasis added.) Comparing the petition filed in IPR2015-01318 and the rehearing request filed by Petitioner in IPR2015-01318, on the one hand, to the Petition filed by Petitioner in this proceeding, on the other hand, with particular focus on the former's discussion of Yamakawa and the latter's

discussion of Hsu, we find that Yamakawa and Hsu are substantially the same insofar as claims 1–8 and 10–15 of the '675 patent are concerned.

In IPR2015-01318, Petitioner asserted that claims 1–8 and 10–15 of the '675 patent are anticipated by Yamakawa. In this proceeding, Petitioner asserts that claims 1–8 and 10–15 of the '675 patent are anticipated by Hsu. Neither assertion is based on any inherency argument, and both assertions rely on a direct reading of each claim limitation onto the prior art. Nothing in either Yamakawa or Hsu had to be specially construed and neither Yamakawa nor Hsu sets forth any special definition of terms. With respect to the challenged claims, we are not cognizant of any necessary disclosure that is provided by Hsu but not Yamakawa. The differences between Hsu and Yamakawa have not been shown to be significant with respect to the challenged claims.

The types of steps said to be disclosed by Hsu are the types of steps said to be disclosed by Yamakawa, and vice versa. If Yamakawa anticipates the challenged claims, it would be expected that the same assertion would be made about Hsu, and the same is true the other way around.

Even Petitioner does not articulate any meaningful difference between the two. Specifically, Petitioner states:

> The first petition relied primarily on the Yamakawa reference. As explained by Dr. Lee, Hsu makes disclosures regarding the portion of third metal gate electrode layer of the PMOS transistor (layer 262 of Hsu) and the upper metal gate electrode (layers 160 and 162 of Hsu) that may be more relevant to the invalidity of the '675 patent. *See* Lee Decl. at ¶ 77. For this reason, while Yamakawa on its own fully anticipates the claims of the '675 patent, Hsu is the stronger reference between the two.

Paper 2, 3. All Petitioner could conclude is that Hsu "may be more relevant." On that non-definitive and general basis, Petitioner states that Hsu is the stronger reference of the two. We are unpersuaded, because Petitioner has not articulated anything sufficiently specific or meaningful in that regard. That Hsu "may be more relevant" also means Yamakawa "may be more relevant." Also, "more or less relevant" is not the test, given that "relevance" is a very broad term. If both Yamakawa and Hsu allegedly anticipate the challenged claims in substantially the same manner, it is inconsequential whether one reference is more or less relevant than the other in some way. Petitioner has provided insufficient support for the bare assertion that Hsu is the stronger reference of the two.

Yamakawa as explained by Petitioner in IPR2015-01318, inclusive of Petitioner's representations in its rehearing request in IPR2015-01318, and Hsu as presented by Petitioner in this proceeding, are substantially the same. Petitioner has not articulated any meaningful difference between the two.

III. CONCLUSION

For the foregoing reasons, we exercise discretion not to institute *inter partes* review of any of claims 1–8 and 10–15 of the '675 patent, and also reject the Petition under 35 U.S.C. § 325(d).

IV. ORDER

It is

ORDERED that no trial or *inter partes* review is instituted for any claim of the '675 patent on any ground.

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